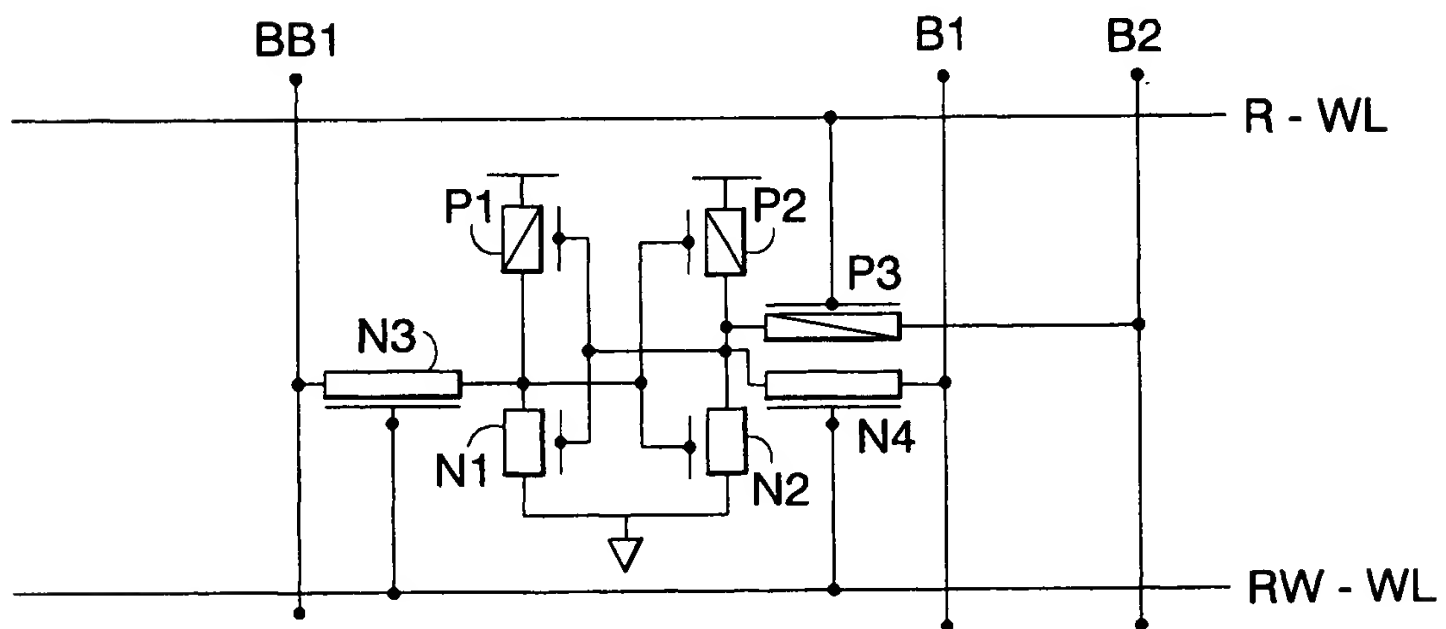


**FIG. 1A**

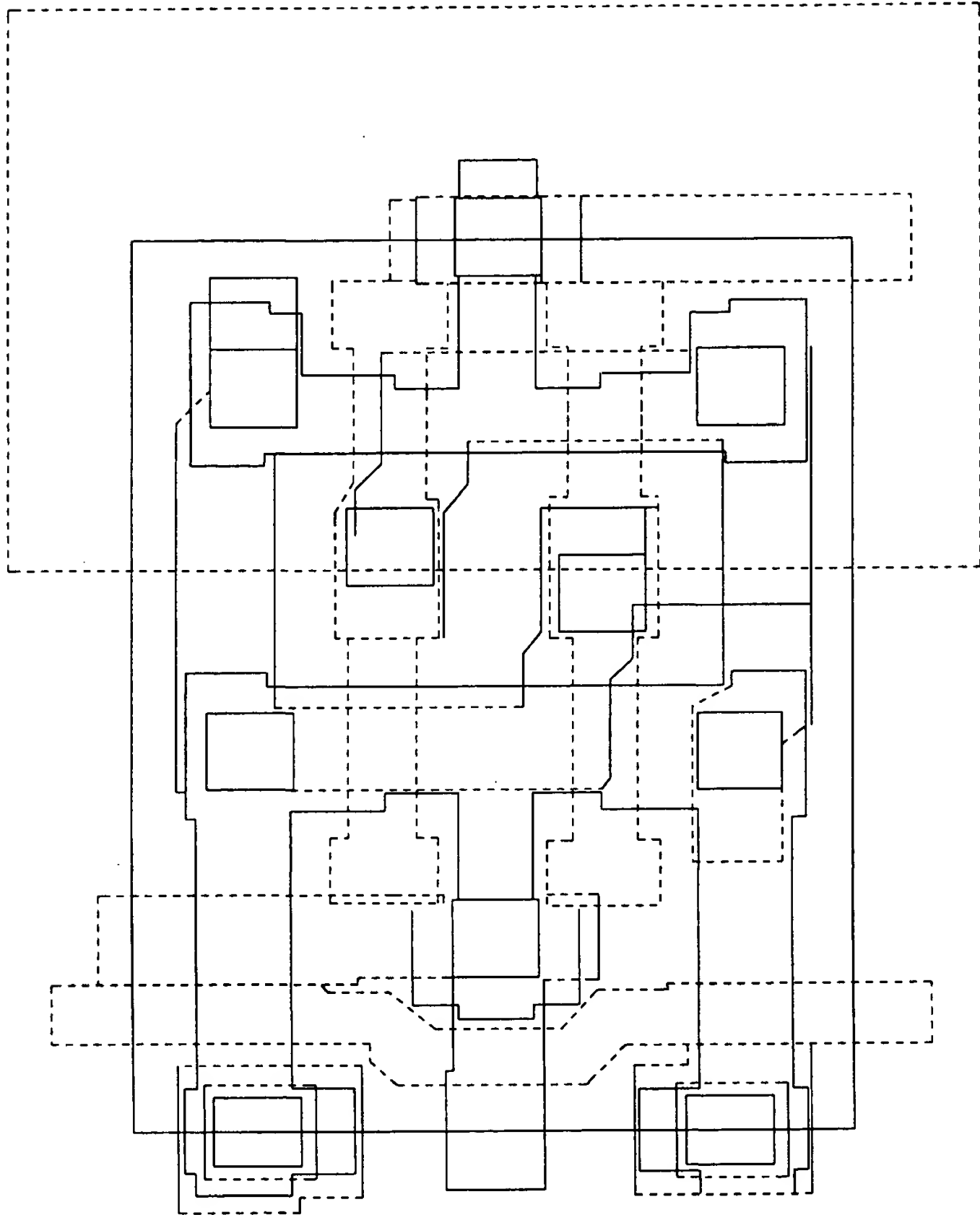


**FIG. 1B**



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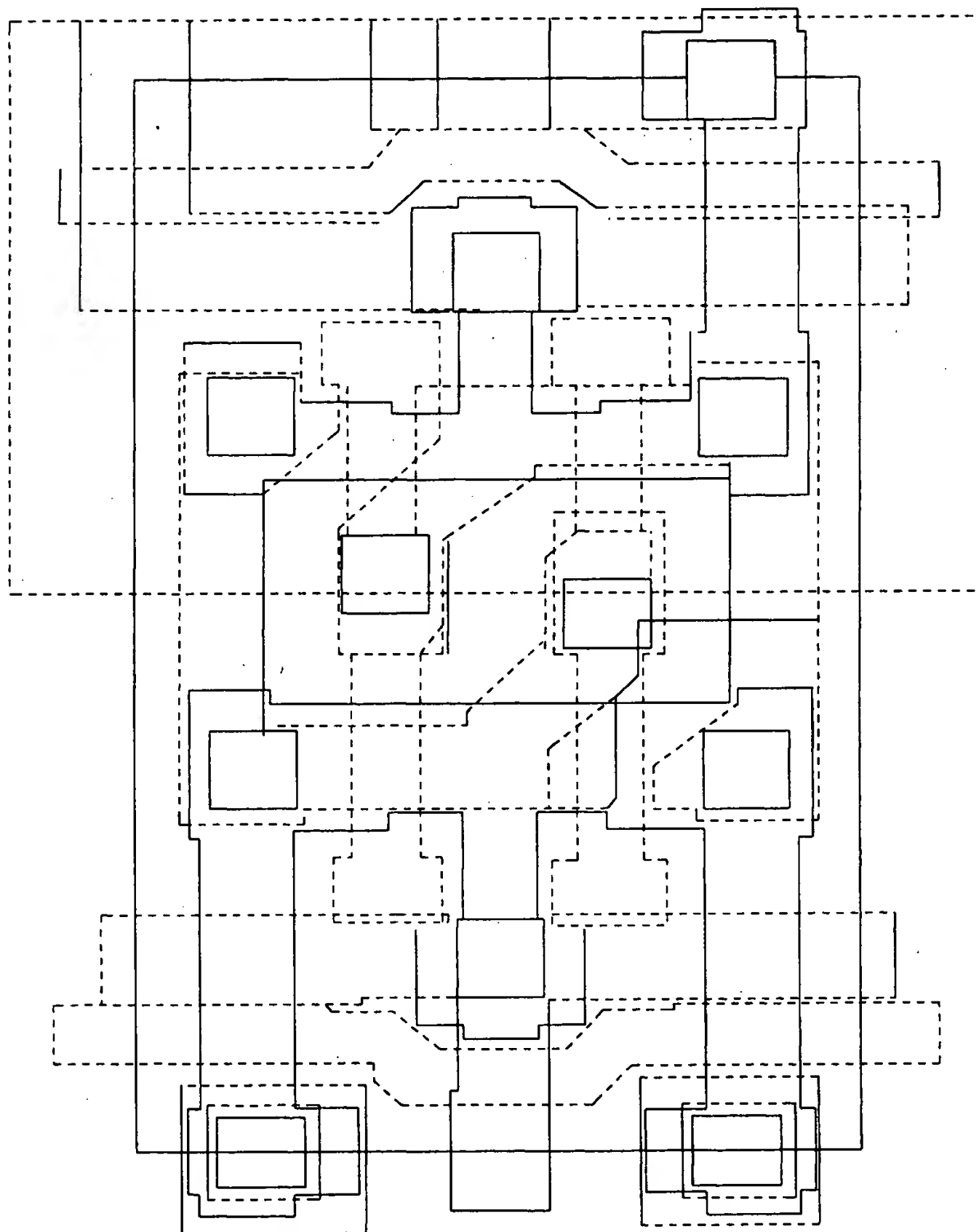
1 Port SRAM Cell  
1.3 x 1.9 - 2.47

**FIG. 1C(1)**  
*(Prior Art)*



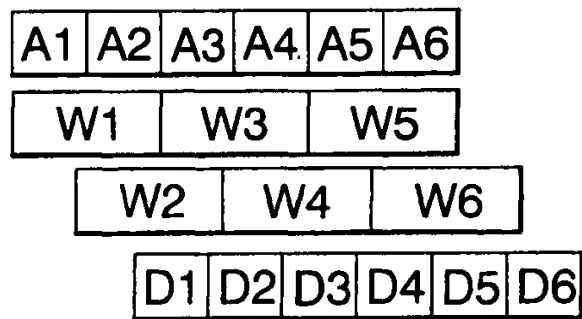
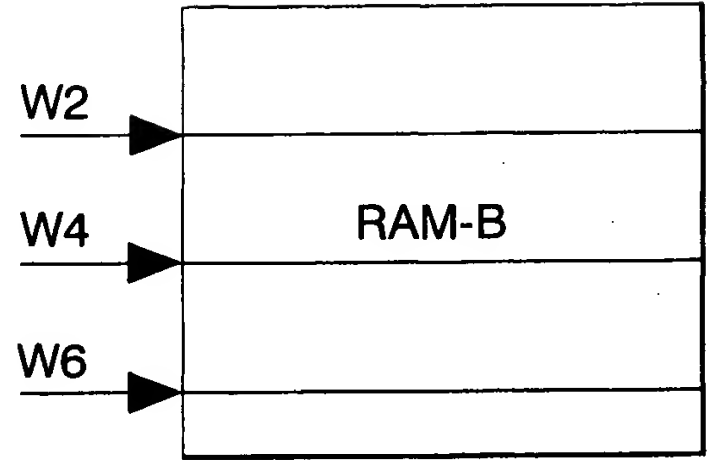
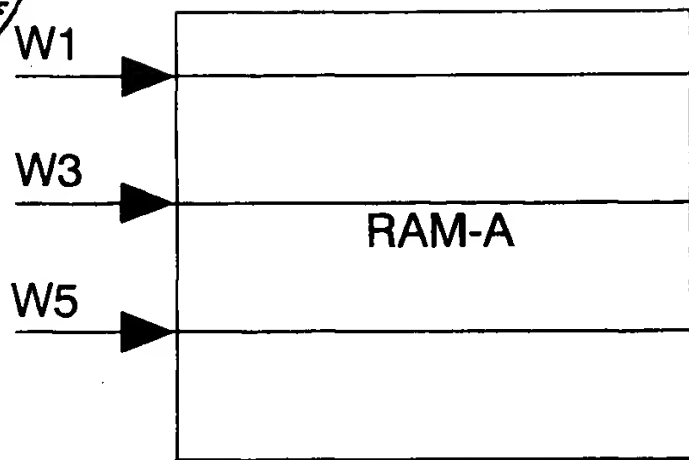
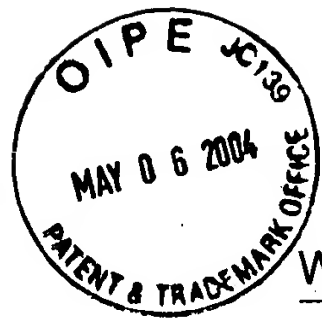
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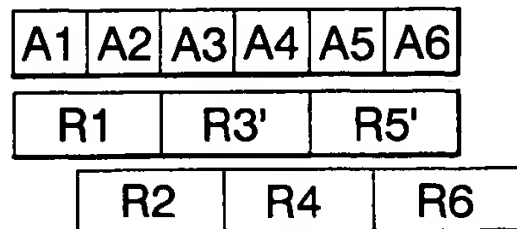
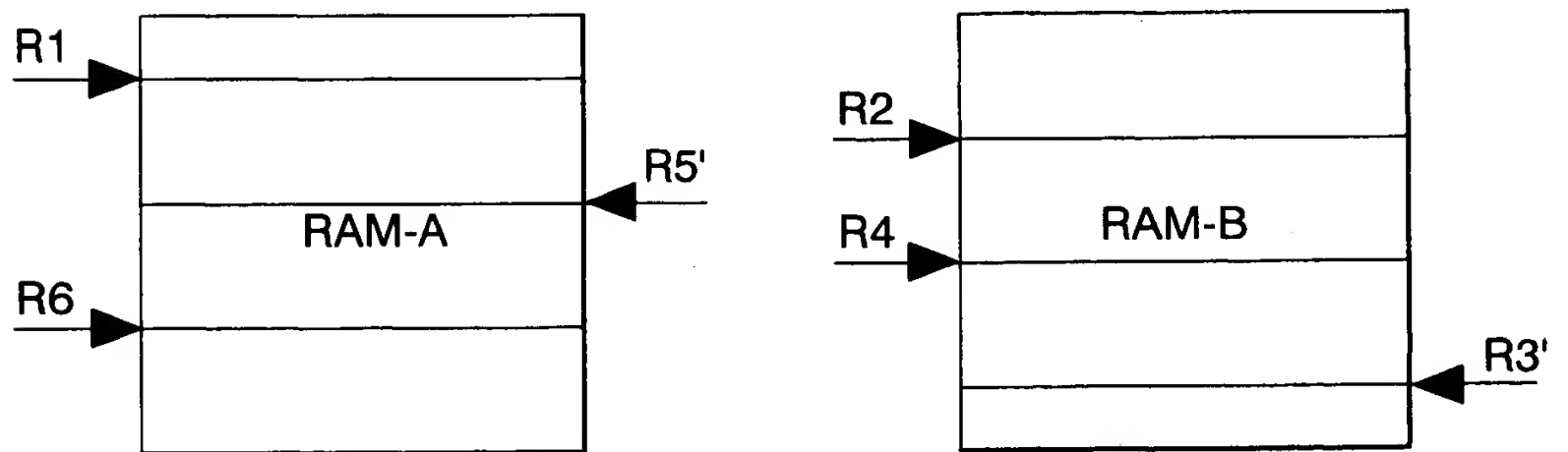
2 Port SRAM Cell  
1.3 x 2.3 - 2.99

**FIG. 1C(2)**



Dual-Port RAM, Interleaved Write Operation

**FIG. 2**



Dual-Port RAM, Interleaved Read Operation

**FIG. 3**